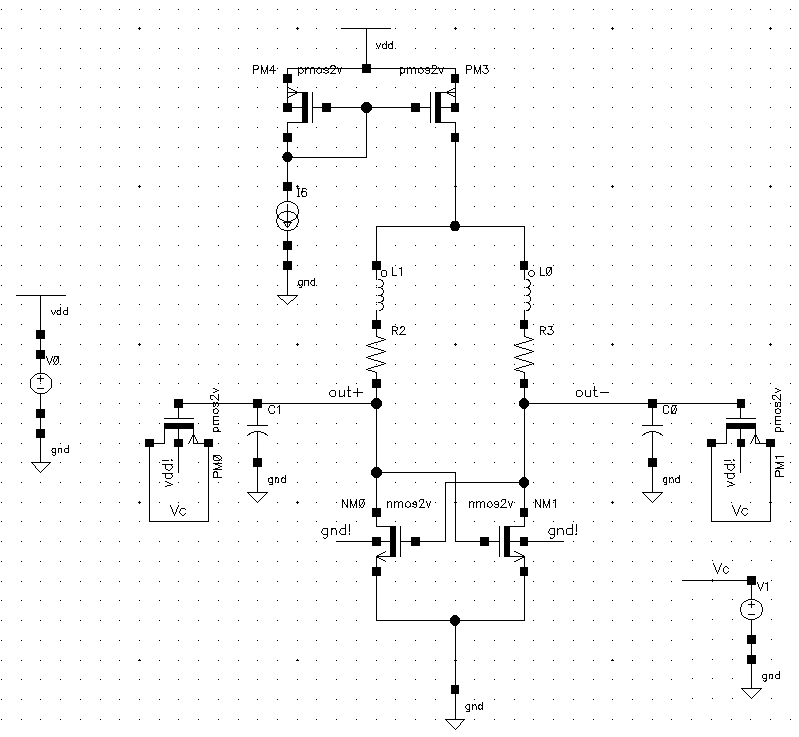
**EE230 – HW2 Report  
CMOS VCO**  
(@ 1.9 GHz & using 45nm CMOS Technology)

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1. **Schematic Setup:**



**Fig. 1. LC VCO schematic**

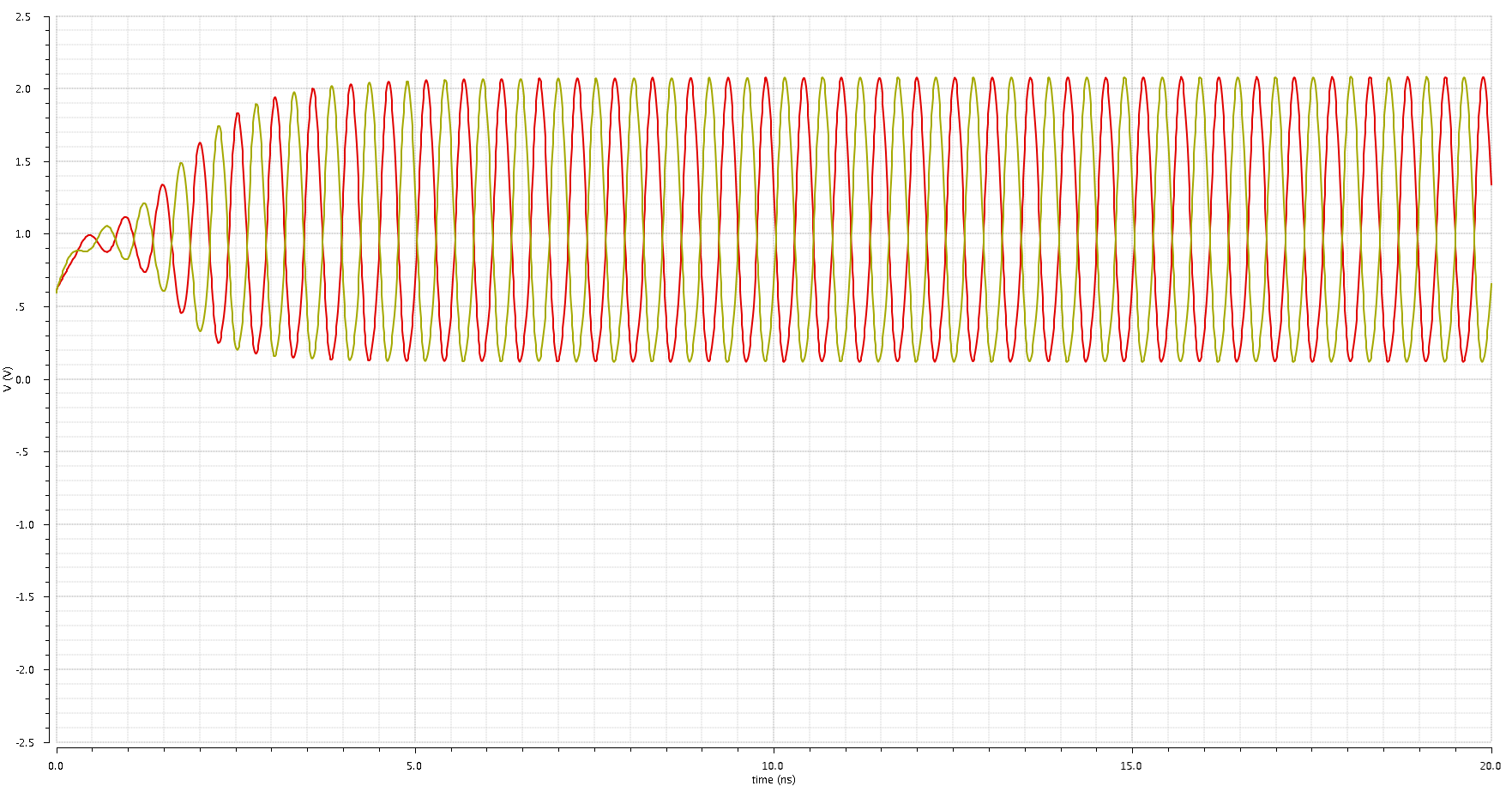
Table 1. Transistor parameters

|  |  |  |  |
| --- | --- | --- | --- |
| Transistor | W [um] | L [um] | Multiplicity |
| NM0, NM1 | 1 | 0.3 | 13 |
| PM0, PM1 | 2 | 1.2 | 12 |
| PM4 | 5 | 1.2 | 1 |
| PM3 | 5 | 1.2 | 24 |

Table 2. Component values

|  |  |
| --- | --- |
| Component | Value |
| L0, L1 | 10 nH |
| R2, R3 | 20 Ohms |
| C0, C1 | 500 fF |
| IBias | 100 uA |
| Vc | 1.3 V |
| VDD | 1.8 V |

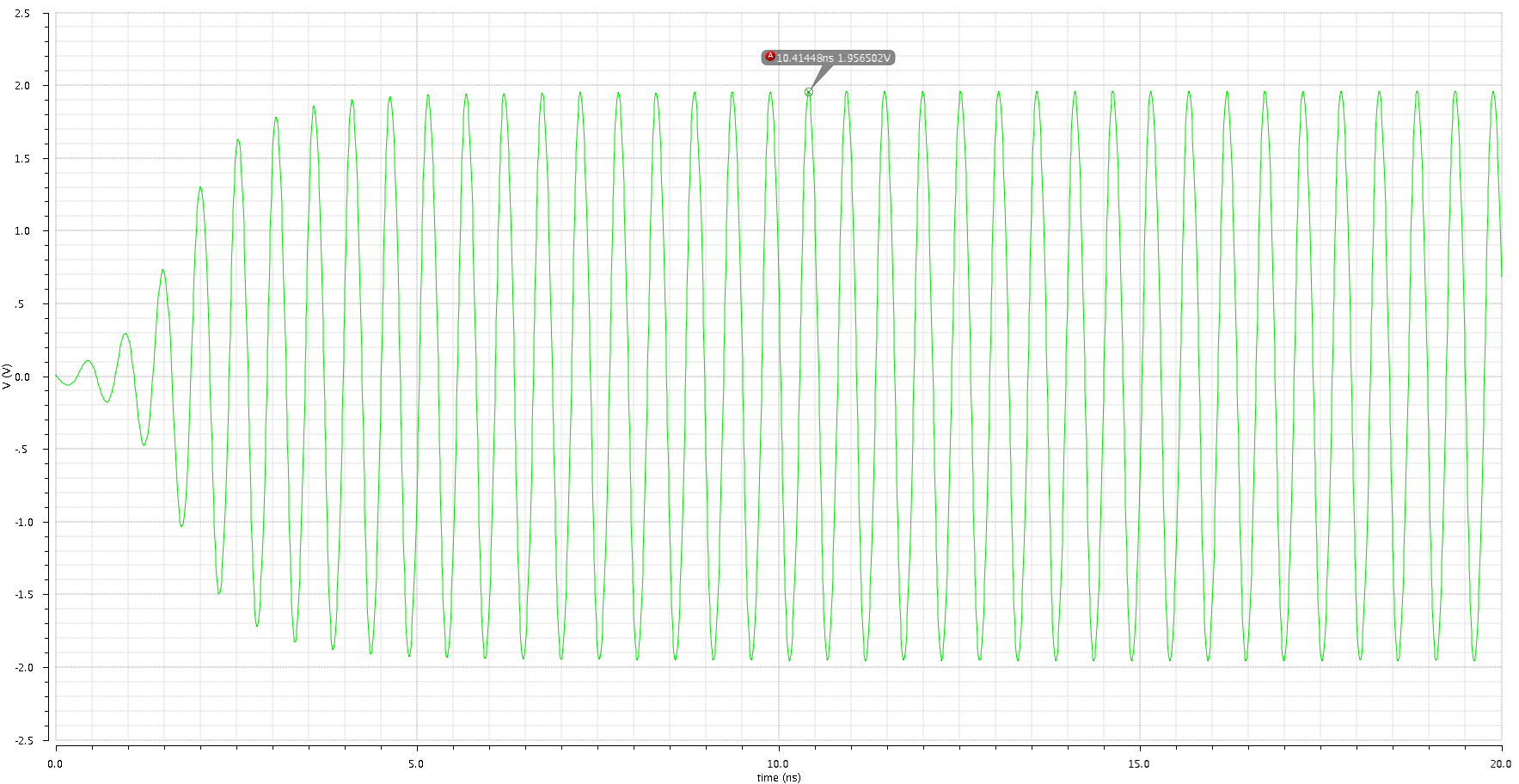
1. **Transient Simulation:**



**Out+**

**Out-**

**Fig. 2. Transient response of the VCO’s single-ended outputs**

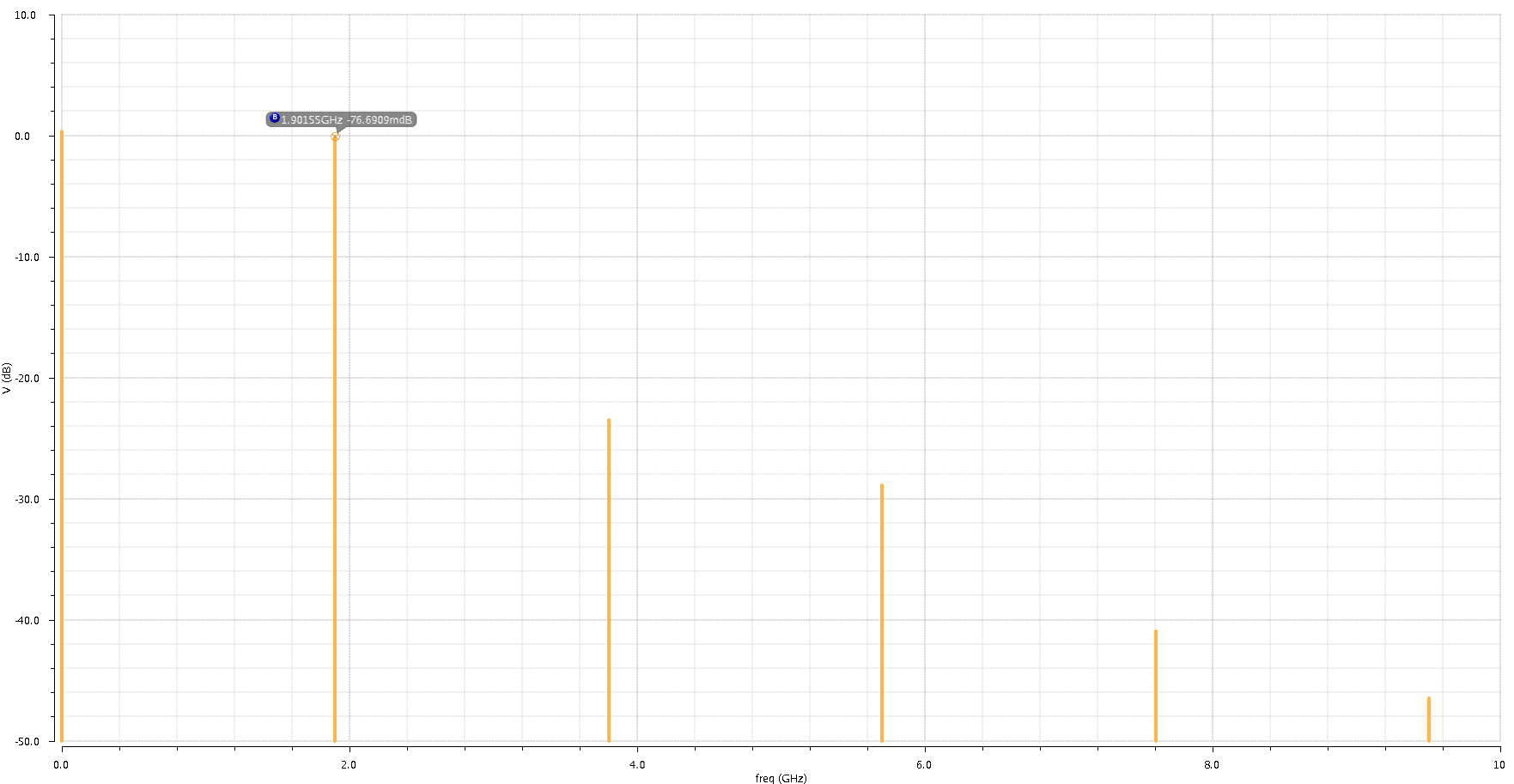


**Diff Output**

**Fig. 3. Transient response of the VCO’s differential output**

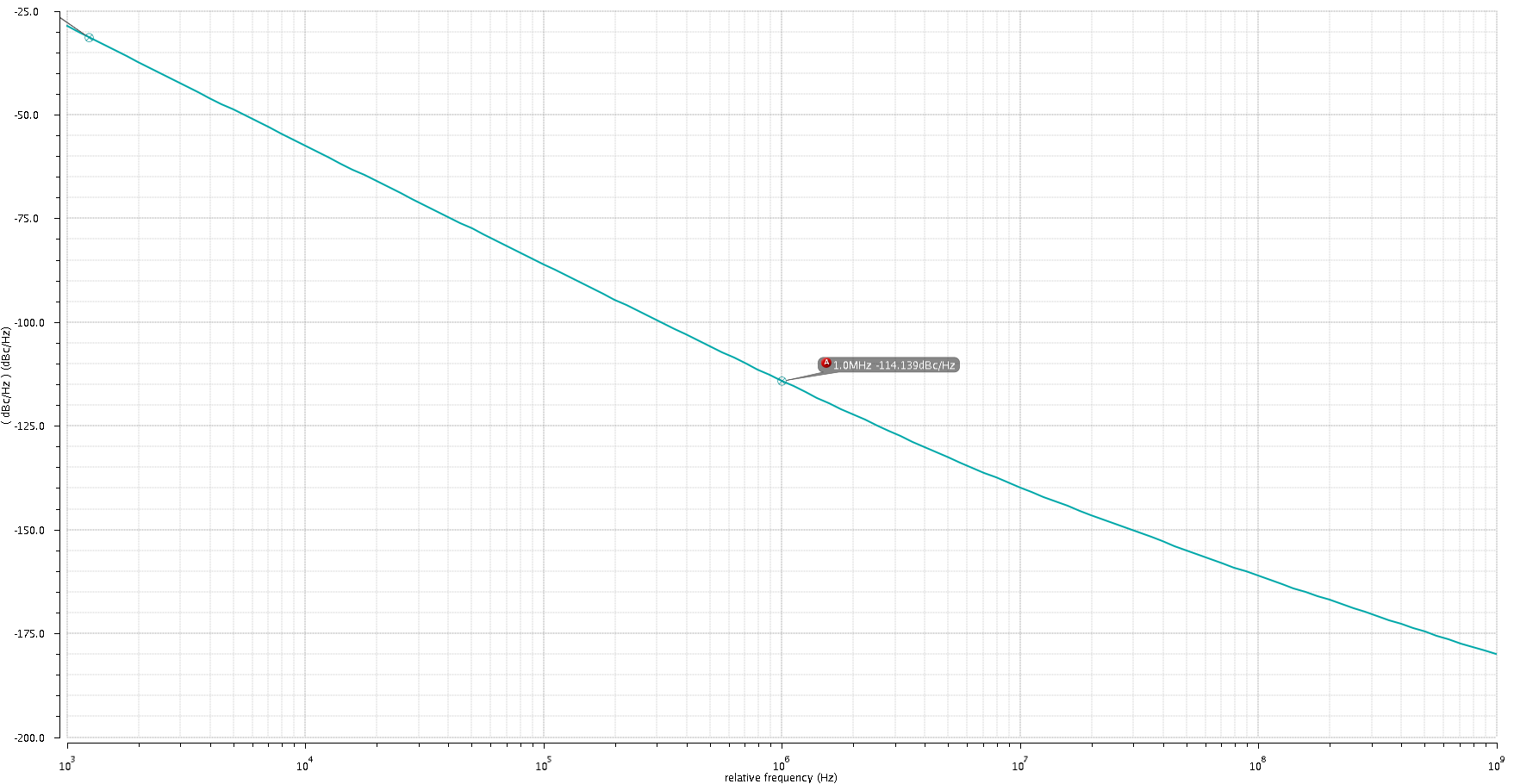
1. **PSS Simulation:**

|  |  |
| --- | --- |
| Parameter | Value @ fo = 1.9GHz |
| Output Spectrum | -0.767 dB |



**Fig. 4. VCO Output Spectrum**

|  |  |
| --- | --- |
| Parameter | Value @ fo = 1.9GHz |
| Phase Noise @ 1MHz offset | -114.14 dBc/Hz |

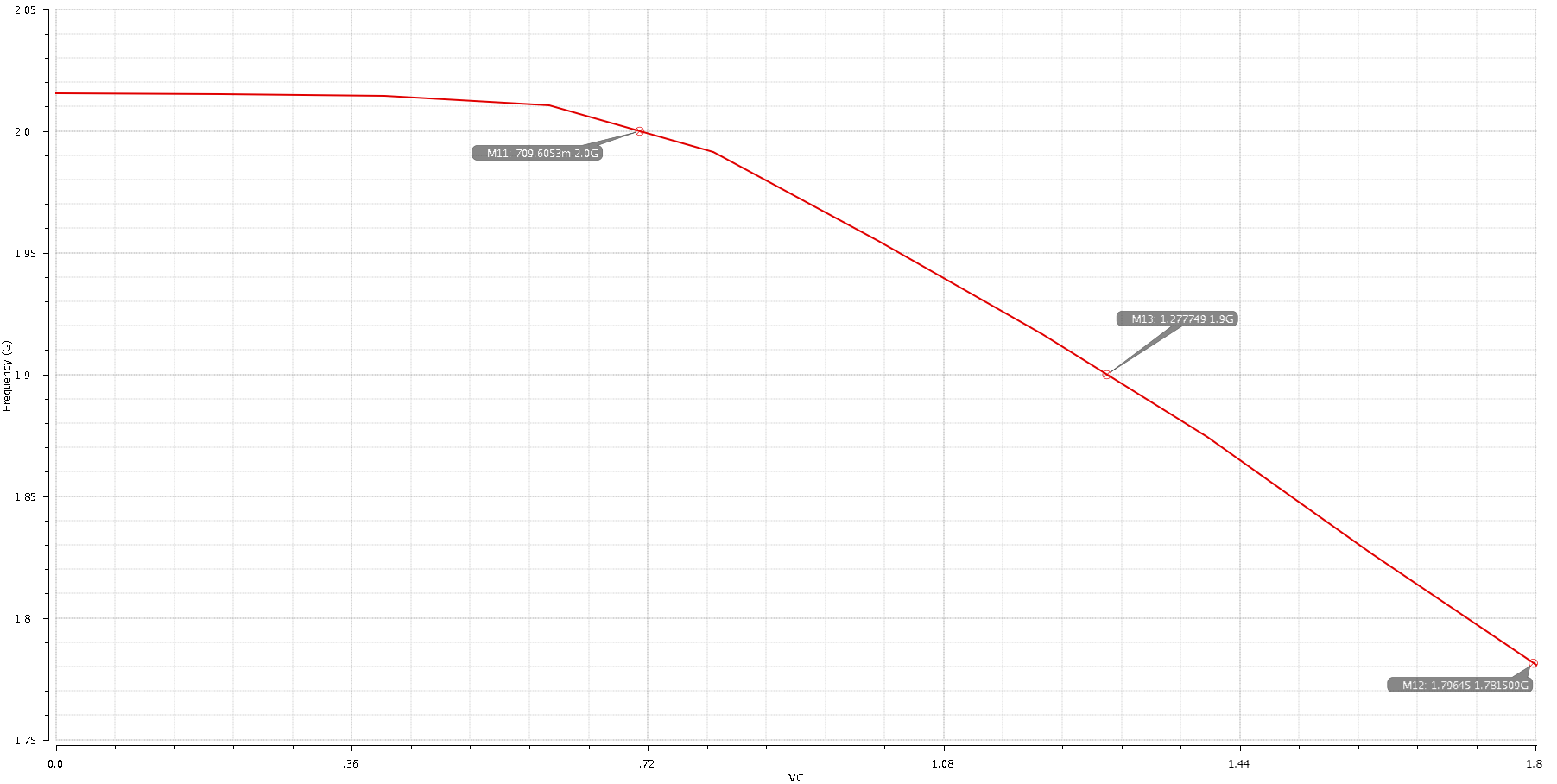


**Fig. 5. VCO Phase Noise**

1. **Parametric Simulation:**

* Freq Vs Vc sweep:

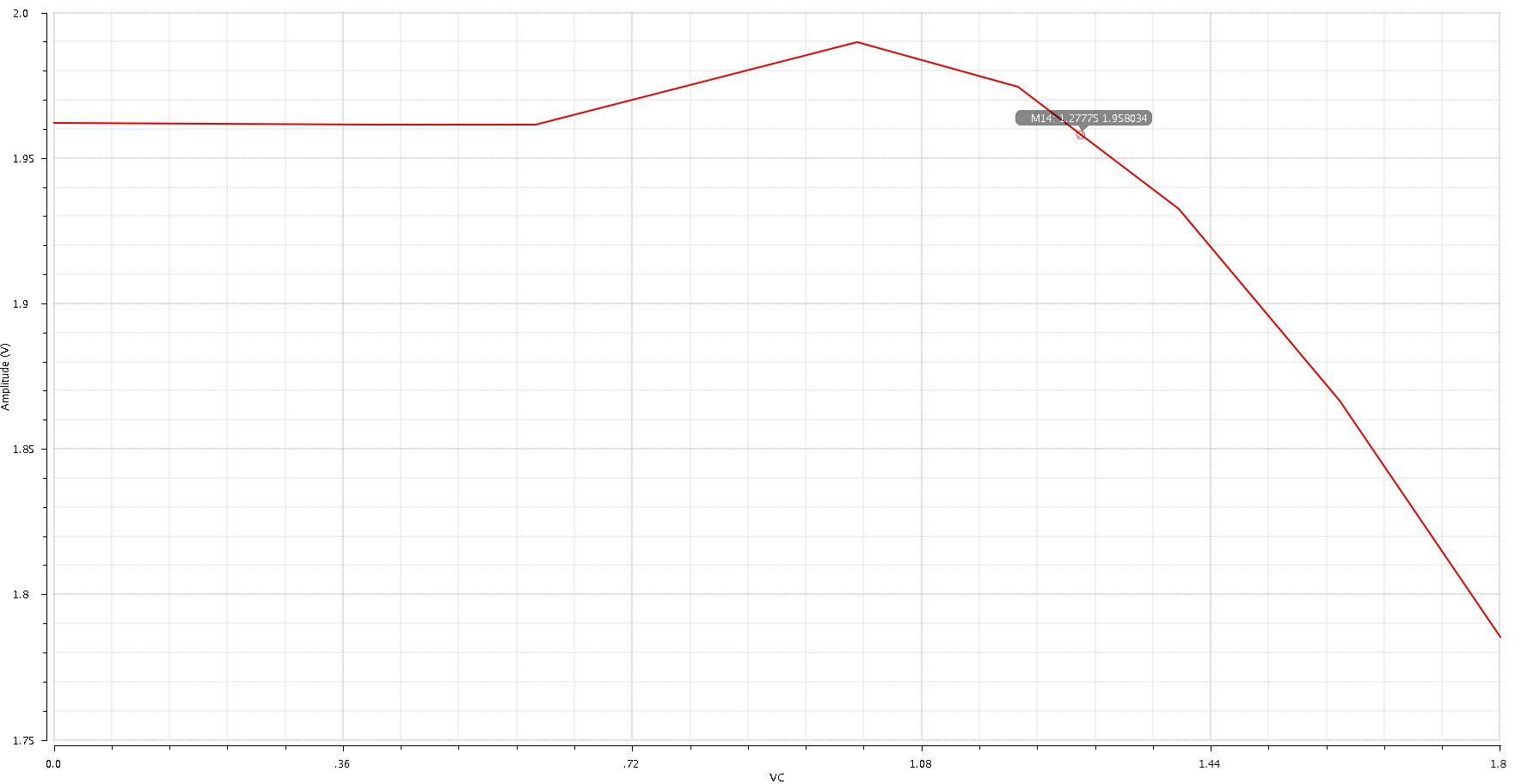
Equation used:  
average(freq(clip((vtime('tran "/out+") - vtime('tran "/out-")) 15n 20n ) "rising" ?xName "time" ?mode "auto" ?threshold 0))



**Fig. 6. Oscillation Frequency Vs Vc**

* Amplitude Vs Vc sweep:

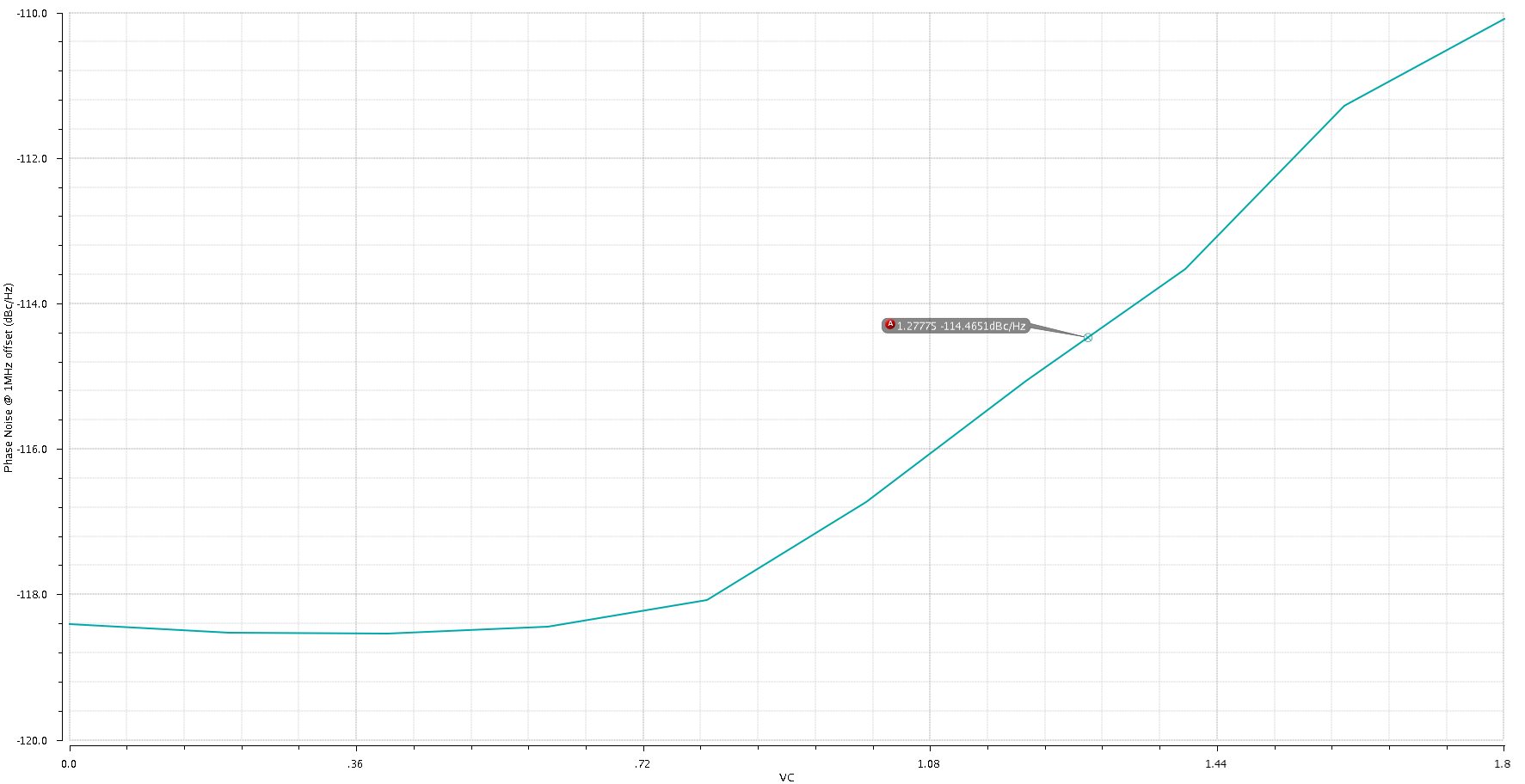
Equation used:  
ymax(clip((vtime('tran "/out+") - vtime('tran "/out-")) 15n 20n ))



**Fig. 7. Output Amplitude Vs Vc**

* Phase Noise Vs Vc sweep:

Equation used:  
value(pn('pnoise) 1M )



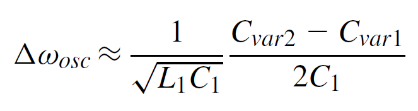
**Fig. 8. Phase Noise at 1MHz offset Vs Vc**

1. **VCO Analysis:**

5.1 Explain the role of varactors on VCO performance such as tuning range, quality factor, linearity of gain, etc.

* The varactor’s main role in the circuit is to provide a variable capacitance to change the frequency of oscillation. Here, a normal inversion-type PMOS is used as a varactor, so increasing Vc from 0 to VDD results in a bigger Cvar that gives a smaller fosc.

Assuming the varactor capacitance range is Cvar2 – Cvar1, the tuning range can be approximated to:



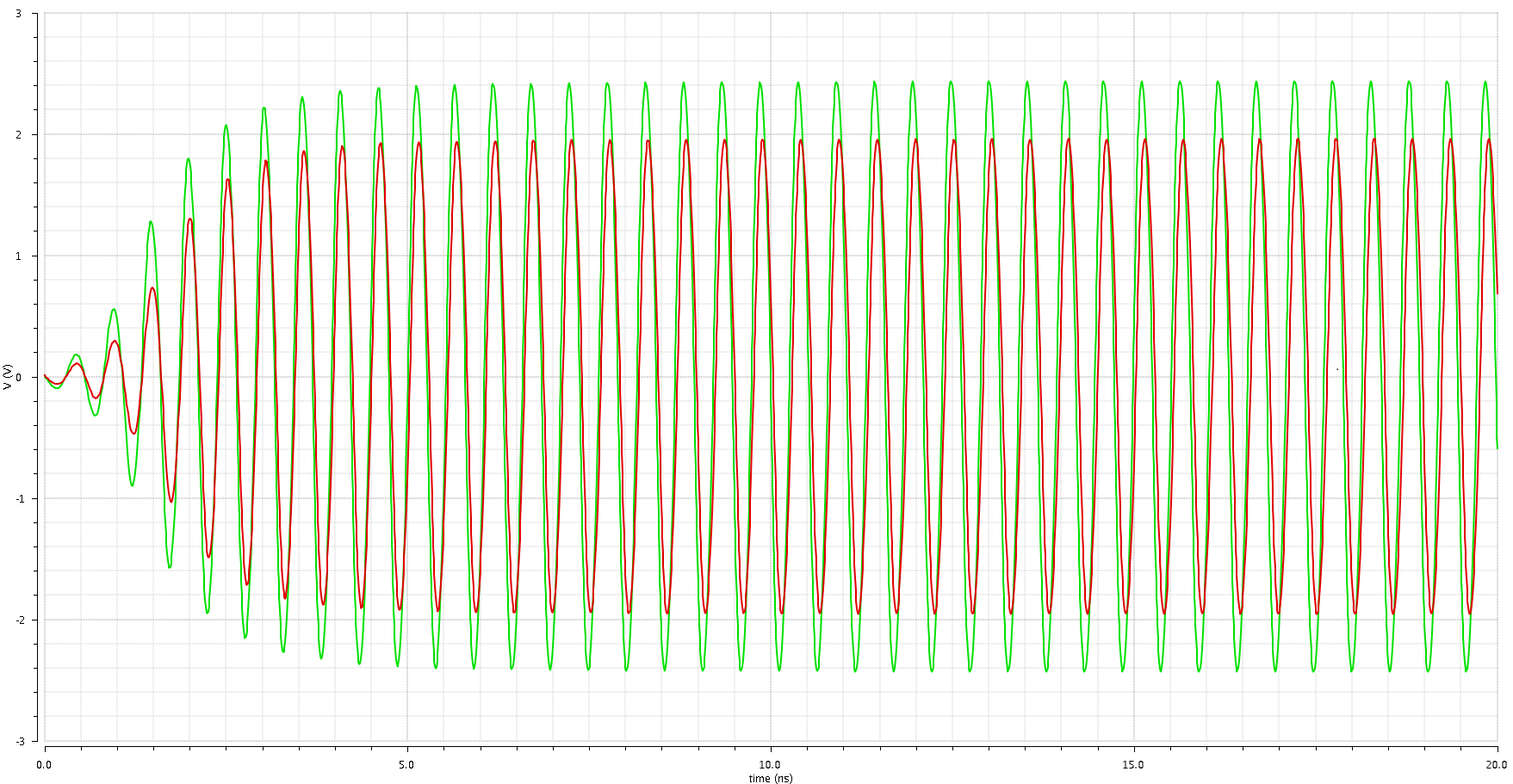
The tuning range trades with the Q of the varactor & the whole tank (hence with the phase noise). Longer channels result in larger range but lower Q. The dimensions of the PMOSs will vary the values of Cvar2 & Cvar1, changing the KVCO.

5.2 Explain how each of the main design variables (bias current, gm of the cross-coupled transistors and Q factor of the LC tank) affect the oscillation amplitude and the phase noise. For a given bias current, what are the trade-offs involved in the choice of the W/L for the nmos transistors?

* The amplitude is increased by increasing IBias & Q, & is decreased by increasing gm (by increasing W/L).
* The phase noise follows an opposite behavior, so it decreases by increasing IBias & Q, & is increased by increasing gm (by increasing W/L).
* For a given bias current, increasing W/L increases gm which in turn causes a faster startup & a higher operating frequency, but a lower amplitude & a higher phase noise.

5.3 Change the Q factor of the modeled inductor from 5 to 9 and obtain parametric plots like the ones shown in section 4. How much does the phase noise change? By how much do you need to change the bias current to obtain the same phase noise as with a Q of 5?

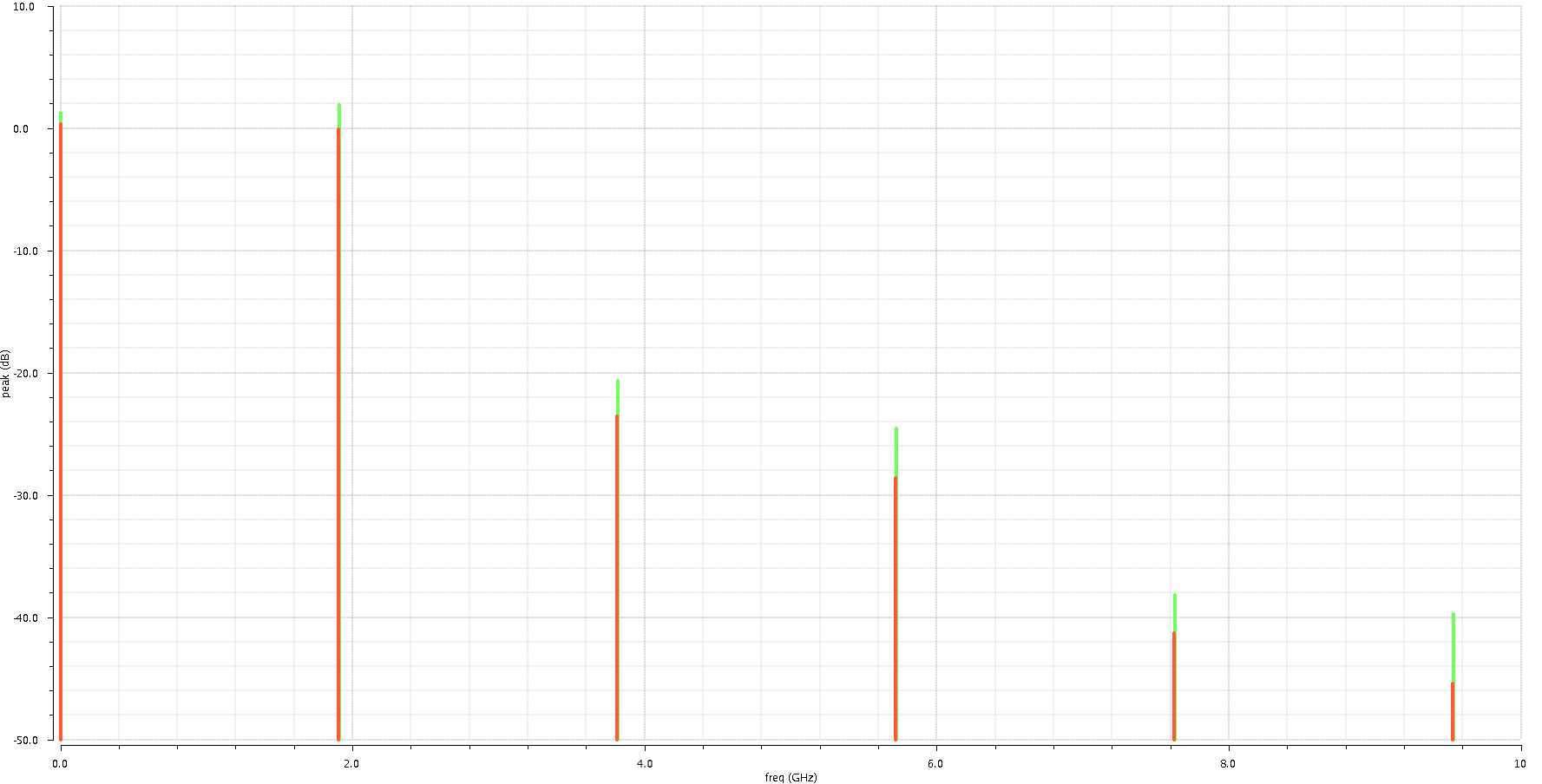
* To change the Q to 9, RS is changed to:



**Q = 9**

**Q = 5**

**Fig. 9. Transient response of the VCO’s differential output at Q = 9 & Q = 5**



**Q = 9**

**Q = 5**

**Fig. 10. VCO Output Spectrum at Q = 9 & Q = 5**



|  |  |  |
| --- | --- | --- |
| Parameter | Q | Value @ fo = 1.9GHz |
| Phase Noise @ 1MHz offset | 5 | -114.14 dBc/Hz |
| 9 | -118.47 dBc/Hz |

**Q = 5**

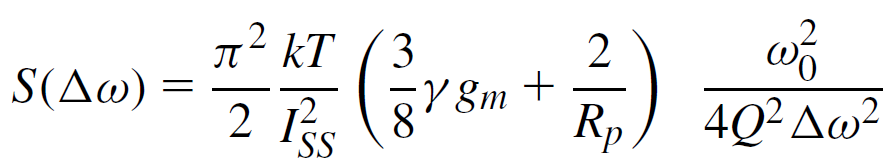
**Q = 9**

**Fig. 11. Phase Noise at Q = 9 & Q = 5**

* For the phase noise at Q=9 to reach that at Q=5, IBias will have to decrease by 0.764 mA. So, with Q=9 & a phase noise -114 dBc/Hz, the power dissipation will decrease to 1.686 mA x 1.8 V = 3.03 mW.

5.4 Measure the Q of the tank. From the measured Q and the gm, and IBias obtained from a DC simulation, estimate the phase noise @1MHz offset. How does this estimation compare with the simulation results?

* , 3.98 mS ,
* The phase noise can be estimated by the following equation:



* The estimated phase noise is lower than the obtained phase noise, which is expected, since we neglected the noise coming from other components, i.e. the varactors & the current tail transistors.

1. **Summary of the results:**

|  |  |
| --- | --- |
| **Parameter** | **Value @ fo = 1.9 GHz** |
| Amplitude | 1.958 V |
| Phase Noise | - 114 dBc/Hz |
| Power Dissipation | 2.45 mA \* 1.8 V = 4.41 mW |
| Tuning Range | 1.781 GHz – 2.015 GHz |